IN THE CLAIMS

Please amend the claims as follows:

1. (Original): A heat-conducting multilayer substrate comprising: at least a Cu circuitry layer of at least 99.999% purity and a ceramic layer.

2. (Original): A heat-conducting multilayer substrate comprising: a ceramic layer, a Cu circuitry layer having at least 99.999% purity provided on one side of said ceramic layer, and a high-purity metal layer provided on the other side of the ceramic layer.

3. (Original): A heat-conducting multilayer substrate according to claim 2, wherein the high-purity metal layer is a Cu metal layer of at least 99.999% purity.

4. (Original): A power module substrate comprising: an insulating substrate, a circuitry layer laminated on one side of said insulating substrate, a metal layer laminated on the other side of said insulating substrate, a semiconductor chip loaded onto the circuitry layer by means of solder, and a radiator joined to the metal layer; wherein, the circuitry layer and the metal layer are composed of copper of at least 99.999% purity.

5. (Original): A power module substrate according to claim 4, wherein the radiator is joined to the metal layer by solder, brazing or a diffused bonding.

6. (Original): A power module substrate according to claim 4, wherein the insulating substrate is composed of AlN, Al_2O_3, Si_3N_4 or SiC.

7. (Original): A power module substrate according to claim 5, wherein the insulating substrate is composed of AlN, Al_2O_3, Si_3N_4 or SiC.

8. (Currently Amended): A power module substrate according to claim 4, wherein the circuitry layer and the metal layer are composed of the copper, which release stress within 24 hours at 100°C.

9. (Currently Amended): A power module substrate according to claim 5, wherein the circuitry layer and the metal layer are composed of the copper, which release stress within 24 hours at 100°C.

10. (Currently Amended): A power module substrate according to claim 6, wherein the circuitry layer and the metal layer are composed of the copper, which release stress within 24 hours at 100°C.

11. (Currently Amended): A power module substrate according to claim 4, wherein ~~elongation during rupture of~~ the circuitry layer and the metal layer are composed of the copper, elongation during rupture of which is from 20% to 30% within the range of -40°C to 150°C.

12. (Currently Amended): A power module substrate according to claim 5, wherein ~~elongation during rupture of~~ the circuitry layer and the metal layer are composed of the copper, elongation during rupture of which is from 20% to 30% within the range of -40°C to 150°C.

13. (Currently Amended): A power module substrate according to claim 6, wherein ~~elongation during rupture of~~ the circuitry layer and the metal layer are composed of the copper, elongation during rupture of which is from 20% to 30% within the range of -40°C to 150°C.

14. (Original): A power module substrate according to claim 4, wherein the thickness of the circuitry layer and the metal layer is from 0.04 mm to 1.0 mm.

15. (Original): A power module substrate according to claim 5, wherein the thickness of the circuitry layer and the metal layer is from 0.04 mm to 1.0 mm.

16. (Original): A power module substrate according to claim 6, wherein the thickness of the circuitry layer and the metal layer is from 0.04 mm to 1.0 mm.

17. (Previously Presented): A power module substrate according to claim 4, wherein the conductivity of the circuitry layer and the metal layer is at least 99% under the International Annealed Copper Standard (IACS).

18. (Currently Amended): A power module substrate according to claim 5, wherein the conductivity of the circuitry layer and the metal layer is at least 99% ~~IACS~~ under the International Annealed Copper Standard (IACS).

19. (Currently Amended): A power module substrate according to claim 6, wherein the conductivity of the circuitry layer and the metal layer is at least 99% ~~IACS~~ under the International Annealed Copper Standard (IACS).

20. (Currently Amended): A power module substrate according to claim 4, wherein [[the]] an average particle diameter of crystalline particles of the circuitry layer and the metal layer is from 1.0 mm to 30 mm.

21. (Currently Amended): A power module substrate according to claim 5, wherein [[the]] an average particle diameter of crystalline particles of the circuitry layer and the metal layer is from 1.0 mm to 30 mm.

22. (Currently Amended): A power module substrate according to claim 6, wherein [[the]] an average particle diameter of crystalline particles of the circuitry layer and the metal layer is from 1.0 mm to 30 mm.